WHAT IS CLAIMED IS:

1. An apparatus comprising:

a first scoreboard;

a second scoreboard; and

a control circuit coupled to the first scoreboard and the second scoreboard, wherein the control circuit is configured to update the first scoreboard to indicate that a write is pending for a first destination register of a first instruction in response to issuing the first instruction into a first pipeline, and wherein the control circuit is configured to update the second scoreboard to indicate that the write is pending for the first destination register in response to the first instruction passing a first stage of the pipeline, wherein replay is signaled at the first stage, and wherein the control circuit, in response to a replay of a second instruction, is configured to copy a contents of the second scoreboard to the first scoreboard.

2. The apparatus as recited in claim 1 further comprising a third scoreboard coupled to the control circuit, wherein the control circuit is configured to update the third scoreboard to indicate that the write is pending for the first destination register in response to the first instruction passing a second stage of the pipeline, wherein an instruction graduates at the second stage, and wherein the control circuit, in response to an exception for a third instruction, is configured to copy a contents of the third scoreboard to the second scoreboard and to the first scoreboard.

3. The apparatus as recited in claim 2 wherein the control circuit is configured to copy

the contents of the third scoreboard to the second scoreboard and to subsequently copy a contents of the second scoreboard to the first scoreboard.

4. The apparatus as recited in claim 1 wherein a redirect due to a mispredicted branch instruction is also detected at the first stage, and wherein the control circuit, in response to the redirect, is configured to copy the contents of the second scoreboard to the first scoreboard.

5. The apparatus as recited in claim 1 wherein the control circuit is configured to detect the replay of the second instruction by checking operands of the second instruction against the second scoreboard.

6. The apparatus as recited in claim 1 wherein the first scoreboard and the second scoreboard track pending writes to integer registers.

7. The apparatus as recited in claim 6 wherein the control circuit is configured to selectively inhibit issuance of a third instruction dependent on which of a plurality of pipelines to which the third instruction is to be issued if the first scoreboard indicates a write pending to one of the operands of the third instruction.

8. The apparatus as recited in claim 7 wherein, if the third instruction is to be issued to a load/store pipeline of the plurality of pipelines, the control circuit is configured to inhibit issuance of the third instruction if the first scoreboard indicates a write pending to one of the operands of the third instruction.

9. The apparatus as recited in claim 8 wherein, if the third instruction is to be issued to an integer pipeline of the plurality of pipelines, the control circuit is configured to allow issuance of the third instruction even if the first scoreboard indicates a write pending to one of the operands of the third instruction.

10. The apparatus as recited in claim 9 wherein the integer pipeline includes a register read stage which is delayed to align the register read stage with a data forwarding stage of the load/store pipeline.

11. The apparatus as recited in claim 6 wherein the first instruction is a load instruction, and wherein the load instruction passes the first stage if the load instruction misses in a data cache.

12. The apparatus as recited in claim 1 wherein the control circuit is configured to update the first scoreboard and the second scoreboard to indicate that the write is not pending to the first destination register at a first predetermined clock cycle prior to the first instruction writing the first destination register.

13. The apparatus as recited in claim 12 further comprising a third scoreboard, wherein the control circuit is configured to update the third scoreboard to indicate that the write is pending to the first destination register in response to issuing the first instruction, and wherein the control circuit is configured to update the third scoreboard to indicate that the write to the first destination register is not pending at a second predetermined clock cycle prior to the first instruction writing the first destination register.

14. The apparatus as recited in claim 13 wherein the second predetermined clock cycle is prior to the first predetermined clock cycle.

15. The apparatus as recited in claim 14 wherein the first scoreboard and the second scoreboard track pending writes to floating point registers, and wherein the control circuit is configured to determine whether or not a floating point multiply-add instruction is issuable by checking the multiplicand operands against the first scoreboard and the add operand against the third scoreboard.

16. The apparatus as recited in claim 14 wherein the control circuit is configured to check for a read after write dependency for an instruction to be issued using the first scoreboard and to check for a write after write dependency using the third scoreboard.

17. The apparatus as recited in claim 13 further comprising a fourth scoreboard, wherein the control circuit is configured to update the fourth scoreboard to indicate the write to the first destination register is pending responsive to the first instruction passing the first stage, and wherein the control circuit is configured to update the fourth scoreboard to indicate that the write to the first destination register is not pending at the second predetermined clock cycle, and wherein the control circuit is configured to copy a contents of the fourth scoreboard to the third scoreboard responsive to the replay of the second instruction.

18. A method comprising:

updating a first scoreboard to indicate that a write is pending for a first destination register of a first instruction in response to issuing the first instruction into a first pipeline;

updating a second scoreboard to indicate that the write is pending for the first destination register in response to the first instruction passing a first stage of the pipeline, wherein replay is signaled at the first stage; and

in response to a replay of a second instruction, copying a contents of the second scoreboard to the first scoreboard.

19. The method as recited in claim 18 further comprising:

updating a third scoreboard to indicate that the write is pending for the first destination register in response to the first instruction passing a second stage of the pipeline, wherein an instruction graduates at the second stage; and

in response to an exception for a third instruction, copying a contents of the third scoreboard to the second scoreboard and to the first scoreboard.

20. The method as recited in claim 19 wherein the copying the contents of the third scoreboard comprises:

copying the contents of the third scoreboard to the second scoreboard; and

subsequently copying a contents of the second scoreboard to the first scoreboard.

21. The method as recited in claim 18 further comprising:

detecting a redirect due to a mispredicted branch instruction at the first stage; and

in response to the redirect, copying the contents of the second scoreboard to the first scoreboard.

22. The method as recited in claim 18 further comprising detecting the replay of the second instruction by checking operands of the second instruction against the second scoreboard.

23. The method as recited in claim 18 wherein the first scoreboard and the second scoreboard track pending writes to integer registers.

24. The method as recited in claim 23 further comprising selectively inhibiting issuance of a third instruction dependent on which of a plurality of pipelines to which the third instruction is to be issued if the first scoreboard indicates a write pending to one of the operands of the third instruction.

25. The method as recited in claim 24 wherein the selectively inhibiting comprises:

if the third instruction is to be issued to a load/store pipeline of the plurality of pipelines, inhibiting issuance of the third instruction if the first scoreboard indicates a write pending to one of the operands of the third instruction; and

if the third instruction is to be issued to an integer pipeline of the plurality of pipelines, allowing issuance of the third instruction even if the first scoreboard indicates a write pending to one of the operands of the third instruction.

26. The method as recited in claim 23 wherein the first instruction is a load instruction, and wherein the load instruction passes the first stage if the load instruction misses in a data cache.

27. The method as recited in claim 18 further comprising updating the first scoreboard and the second scoreboard to indicate that the write is not pending to the first destination register at a first predetermined clock cycle prior to the first instruction writing the first destination register.

28. The method as recited in claim 27 further comprising:

updating a third scoreboard to indicate that the write is pending to the first

destination register in response to issuing the first instruction; and

updating the third scoreboard to indicate that the write to the first destination register is not pending at a second predetermined clock cycle prior to the first instruction writing the first destination register.

29. The method as recited in claim 28 wherein the second predetermined clock cycle is prior to the first predetermined clock cycle.

30. The method as recited in claim 29 wherein the first scoreboard and the second scoreboard track pending writes to floating point registers, the method further comprising determining whether or not a floating point multiply-add instruction is issuable by checking the multiplicand operands against the first scoreboard and the add operand against the third scoreboard.

31. The method as recited in claim 29 further comprising:

checking for a read after write dependency for an instruction to be issued using the first scoreboard; and

checking for a write after write dependency using the third scoreboard.

32. The method as recited in claim 28 further comprising:

updating a fourth scoreboard to indicate the write to the first destination register is pending responsive to the first instruction passing the first stage;

updating the fourth scoreboard to indicate that the write to the first destination register is not pending at the second predetermined clock cycle; and

copying a contents of the fourth scoreboard to the third scoreboard responsive to the replay of the second instruction.

33. A carrier medium comprising one or more data structures representing:

a first scoreboard;

a second scoreboard; and

a control circuit coupled to the first scoreboard and the second scoreboard, wherein the control circuit is configured to update the first scoreboard to indicate that a write is pending for a first destination register of a first instruction in response to issuing the first instruction into a first pipeline, and wherein the control circuit is configured to update the second scoreboard to indicate that the write is pending for the first destination register in response to the first instruction passing a first stage of the pipeline, wherein replay is signaled at the first stage, and wherein the control circuit, in response to a replay of a second instruction, is configured to copy a contents of the second scoreboard to the first scoreboard.